

# We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

4,800

Open access books available

122,000

International authors and editors

135M

Downloads

Our authors are among the

154

Countries delivered to

TOP 1%

most cited scientists

12.2%

Contributors from top 500 universities



WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index  
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?  
Contact [book.department@intechopen.com](mailto:book.department@intechopen.com)

Numbers displayed above are based on latest data collected.  
For more information visit [www.intechopen.com](http://www.intechopen.com)



# Analysis of Parasitic Effects in AlGaIn/GaN HEMTs

Kazushige Horio  
Shibaura institute of Technology  
Japan

## 1. Introduction

AlGaIn/GaN high electron mobility transistors (HEMTs) are now receiving great attention because of their potential applications to high-power and high-frequency devices (Mishra et al., 2008). An output power of more than 32 W/mm is reported at 4 GHz for the 0.55  $\mu\text{m}$  gate-length device (Wu et al., 2004), and a current-gain cutoff frequency ( $f_T$ ) of 163 GHz is obtained for 0.06  $\mu\text{m}$  gate length (Higashiwaki et al., 2006). However, slow current transients are often observed even if the gate voltage or the drain voltage is changed abruptly (Binari et al., 2002). This is called gate lag or drain lag, and is problematic in circuit applications. The slow transients indicate that the dc current-voltage ( $I$ - $V$ ) curves and the RF  $I$ - $V$  curves become quite different, resulting in lower RF power available than that expected from the dc operation (Binari et al., 2002; Mishra et al., 2008). This is called power slump or current collapse. This current reduction in RF  $I$ - $V$  curves or pulsed  $I$ - $V$  curves is also referred to as current slump, RF dispersion and knee-walkout behavior. These parasitic effects are serious problems, and there are many experimental works reported on these phenomena (Khan et al., 1994; Daumiller et al., 2001; Ventury et al., 2001; Koley et al., 2003; Mizutani et al., 2003; Koudymov et al., 2003; Meneghesso et al., 2004; Desmaris et al., 2006), but, only a few theoretical works are reported recently (Braga et al., 2004; Meneghesso et al., 2004; Tirado et al., 2007). The literature suggests that the surface properties (surface states) play an important role in these phenomena, but traps in a buffer layer could also affect the characteristics (Binari et al., 2002; Desmaris et al., 2006). It is also shown that the gate lag and current collapse can be reduced by introducing a field plate (Koudymov et al., 2005). This is considered due to a decrease in surface-state effects. It is well recognized that the field plate can improve the breakdown voltage and the power performance, because the electric field at the drain edge of the gate is reduced (Karmalkar & Mishra, 2001; Ando et al., 2003; Xing et al., 2004; Saito et al., 2005; Pala et al., 2008). However, it is not well understood whether the field plate affects buffer-related lag phenomena and current collapse.

In the previous theoretical works by device simulation, effects of a donor-type surface state (near the valence band) on gate lag and pulsed  $I$ - $V$  curves of AlGaIn/GaN HEMTs were studied (Meneghesso et al., 2004; Tirado et al., 2007), and a bulk deep-acceptor effect ( $\sim 1$  eV) above the midgap of GaN was studied for the gate lag (Braga et al., 2004). However, the types of traps and their energy levels seem to be artificial. Therefore, in this article, we have

made two-dimensional transient simulations of AlGaIn/GaN HEMTs with a buffer layer in which trap levels based on experiments are considered, as in our previous work on GaN MESFETs (Horio et al, 2005), and showed that the lag phenomena and current collapse could be reproduced (Horio & Nakajima, 2008). Also, we have studied dependence of current collapse on the impurity densities in the buffer layer and on an off-state drain voltage. Additionally, we have analyzed effects of introducing a field plate on buffer-related lag phenomena and current collapse (Nakajima et al., 2009).

In Section 2, we describe physical models used here, such as analyzed device structures, traps in the buffer layer, and basic equations for the device analysis. Calculated drain-current responses are described in section 3 in terms of drain lag, gate lag and pulsed  $I$ - $V$  curves (current collapse). The dependence of current collapse on the impurity densities in the buffer layer and on an off-state drain voltage is also described. In section 4, effects of introducing a field plate on buffer-related lag phenomena and current collapse are described.

## 2. Physical Model

Fig.1 shows modeled AlGaIn/GaN HEMT structures analyzed in this study. Fig.1(a) is a normal structure without a field plate, and Fig.1(b) is a structure with a field plate. The gate length  $L_G$  is  $0.3\ \mu\text{m}$ , and the source-to-gate distance  $L_{SG}$  is  $0.5\ \mu\text{m}$ . The gate-to-drain distance  $L_{GD}$  is typically set to  $1\ \mu\text{m}$  in Fig.1(a) and  $1.5\ \mu\text{m}$  in Fig.1(b). Note that in Fig.1(b), the gate electrode extends on to SiN passivation layer. This is called field plate. The field-plate length  $L_{FP}$  is typically set to  $1\ \mu\text{m}$ . The thickness of SiN layer  $d$  is varied as a parameter between 0 and  $0.1\ \mu\text{m}$ . Polarization charges of  $10^{13}\ \text{cm}^{-2}$  are set at the heterojunction interface, and the surface polarization charges are assumed to be compensated by surface-state charges, as in (Karmalkar & Mishra, 2001). As a model for the buffer layer, we use a three level compensation model which includes a shallow donor, a deep donor and a deep acceptor (Horio et al., 2005). Some representative experiments show that two levels ( $E_C - 1.8\ \text{eV}$ ,  $E_C - 2.85\ \text{eV}$ ) are associated with current collapse in GaN-based FETs with a semi-insulating buffer layer (Klein et al., 1999; Binari et al., 2002). Therefore, we use an energy level of  $E_C - 2.85\ \text{eV}$  ( $E_V + 0.6\ \text{eV}$ ) for the deep acceptor, and for convergence problem, we use  $E_C - 1.7\ \text{eV}$  for the deep donor. (Note that the origin of these deep levels is not well known and our treatment is only an assumption.) Other experiments show shallower energy levels for deep

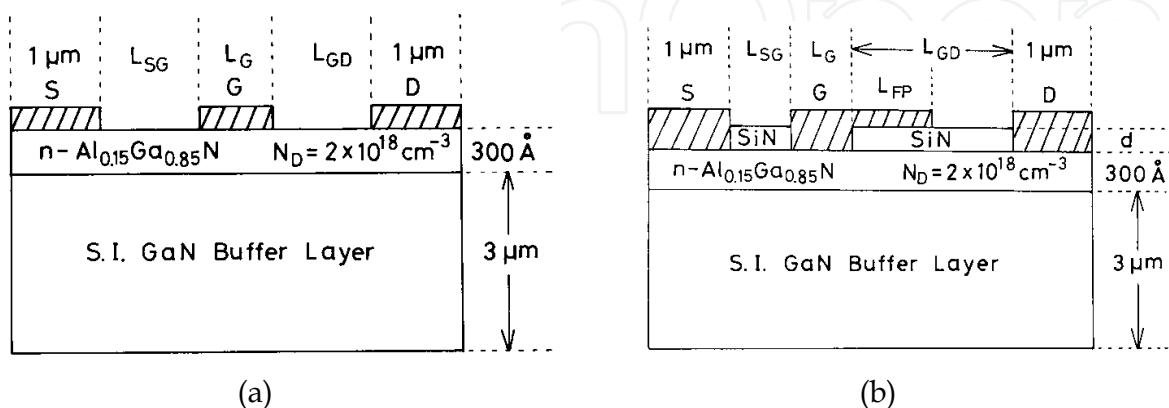


Fig. 1. Modeled AlGaIn/GaN HEMT structures analyzed here. (a) normal structure without a field plate. (b) structure with a field plate

donors in AlGaIn/GaN system or in GaN (Kruppa et al., 1995; Morkoc, 1999), so that we vary the deep donor's energy level ( $E_{DD}$ ) as a parameter. Here, the deep-donor density ( $N_{DD}$ ) and the deep-acceptor density ( $N_{DA}$ ) are typically set to  $5 \times 10^{16} \text{ cm}^{-3}$  and  $2 \times 10^{16} \text{ cm}^{-3}$ , respectively. The electron and hole capture cross sections for the deep donor are set to  $10^{-13} \text{ cm}^2$  and  $10^{-15} \text{ cm}^2$ , respectively, and the electron and hole capture cross sections for the deep acceptor are both set to  $10^{-15} \text{ cm}^2$ . The shallow-donor density in the buffer layer  $N_{Di}$  is set to  $10^{15} \text{ cm}^{-3}$ . Here, it should be noted that when  $N_{DD} > N_{DA}$ , the deep acceptors are usually fully occupied by electrons that are supplied from the deep donors, and the ionized (empty) deep donors act as electron traps (the ionized deep-donor density  $N_{DD}^+$  is nearly equal to  $N_{DA}$  under equilibrium).

Basic equations to be solved are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels (Horio et al., 2000; Horio et al., 2005). They are expressed as follows.

1) Poisson's equation

$$\nabla \cdot (\epsilon \nabla \psi) = -q(p - n + N_D + N_{Di} + N_{DD}^+ - N_{DA}^-) \quad (1)$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - (R_{n,DD} + R_{n,DA}) \quad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - (R_{p,DD} + R_{p,DA}) \quad (3)$$

where

$$R_{n,DD} = C_{n,DD} N_{DD}^+ n - e_{n,DD} (N_{DD} - N_{DD}^+) \quad (4)$$

$$R_{n,DA} = C_{n,DA} (N_{DA} - N_{DA}^-) n - e_{n,DA} N_{DA}^- \quad (5)$$

$$R_{p,DD} = C_{p,DD} (N_{DD} - N_{DD}^+) p - e_{p,DD} N_{DD}^+ \quad (6)$$

$$R_{p,DA} = C_{p,DA} N_{DA}^- p - e_{p,DA} (N_{DA} - N_{DA}^-) \quad (7)$$

3) Rate equations for the deep levels

$$\frac{\partial}{\partial t} (N_{DD} - N_{DD}^+) = R_{n,DD} - R_{p,DD} \quad (8)$$

$$\frac{\partial}{\partial t} N_{DA}^- = R_{n,DA} - R_{p,DA} \quad (9)$$

where  $N_{DD}^+$  and  $N_{DA}^-$  represent ionized densities of the deep donors and the deep acceptors, respectively.  $C_n$  and  $C_p$  are the electron and hole capture coefficients of the deep levels, respectively,  $e_n$  and  $e_p$  are the electron and hole emission rates of the deep levels, respectively, and the subscript (DD, DA) represents the corresponding deep level.

The above basic equations are put into discrete forms, and are solved numerically. We have calculated drain-current responses of the AlGaIn/GaN HEMTs when the drain voltage and/or the gate voltage are changed abruptly.

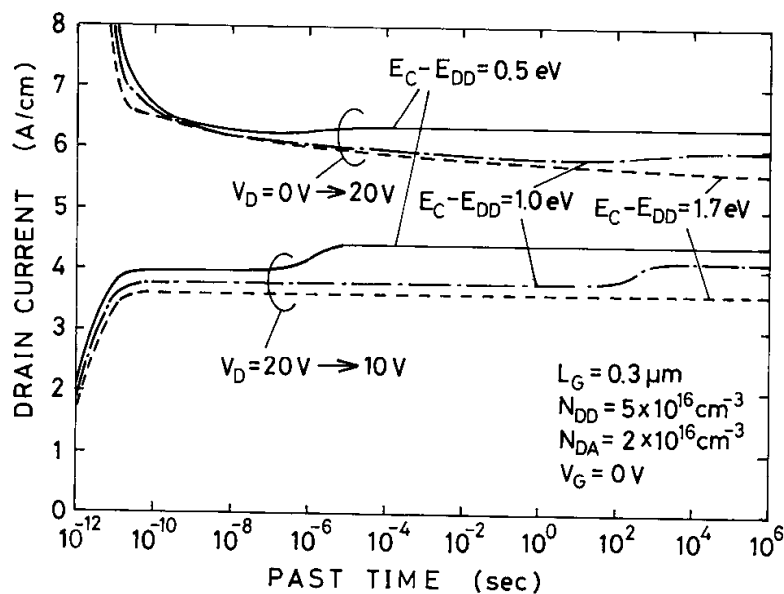


Fig. 2. Calculated drain-current responses of normal AlGaIn/GaN HEMTs as a parameter of deep donor's energy level  $E_{DD}$  when  $V_D$  is raised abruptly from 0 V to 20 V (upper) or when  $V_D$  is lowered from 20 V to 10 V (lower).  $V_G = 0$  V.  $L_{GD} = 1$   $\mu\text{m}$ ,  $N_{DD} = 5 \times 10^{16} \text{ cm}^{-3}$  and  $N_{DA} = 2 \times 10^{16} \text{ cm}^{-3}$ .

### 3. Parasitic Effects in AlGaIn/GaN HEMTs

#### 3.1 Drain lag

First, we describe a case when only the drain voltage  $V_D$  is changed. Fig.2 shows calculated drain-current responses of normal AlGaIn/GaN HEMTs when  $V_D$  is raised abruptly from 0 V to 20 V (upper) or when it is lowered abruptly from 20 V to 10 V (lower), where the gate voltage ( $V_G$ ) is kept constant at 0 V. Here  $N_{DD}$  is  $5 \times 10^{16} \text{ cm}^{-3}$  and  $N_{DA}$  is  $2 \times 10^{16} \text{ cm}^{-3}$ , and three cases with different  $E_C - E_{DD}$  are shown. In the cases when  $V_D$  is raised, initially an extremely large transient overshoot is observed (Horio and Fuseya, 1994). This is because the drain voltage is initially applied along the gate-to-drain bulk region. This initial current decays as the space-charge region at the gate edge extends toward the drain. After this extreme overshoot, the drain currents decrease gradually, reaching steady-state values, although slight undershoot is observed just before reaching the steady state for  $E_C - E_{DD} = 0.5$  eV and 1.0 eV. On the other hand, when  $V_D$  is lowered, initially a large transient undershoot is observed. This is also due to the abrupt change of drain voltage, as described above (Horio and Fuseya, 1994). Then, the drain currents remain at low values for some periods ("quasi-steady state") and begin to increase slowly, showing drain-lag behavior. The response is faster for shallower  $E_{DD}$ , and for  $E_C - E_{DD} = 1.7$  eV, the drain current  $I_D$  remains at a low value even at  $10^6$  s. The change of drain current ( $\Delta I_D$ ) between the quasi-steady state and the steady state is not so dependent on  $E_C - E_{DD}$ .

Fig.3 and Fig.4 show electron density profiles and ionized deep-donor density  $N_{DD}^+$  profiles, respectively, as a function of time  $t$  when  $V_D$  is raised from 0 V to 20 V, where  $E_C - E_{DD} = 1.0$  eV. From Fig.3(b), we can see that electrons are injected into the buffer layer when  $V_D$  is raised, and at this time ( $t = 10^{-10}$  s), the deep donors are not almost responding (see Figs.4(a) and (b)). It is understood that  $I_D$  decreases due to electron capturing by the deep donors. In

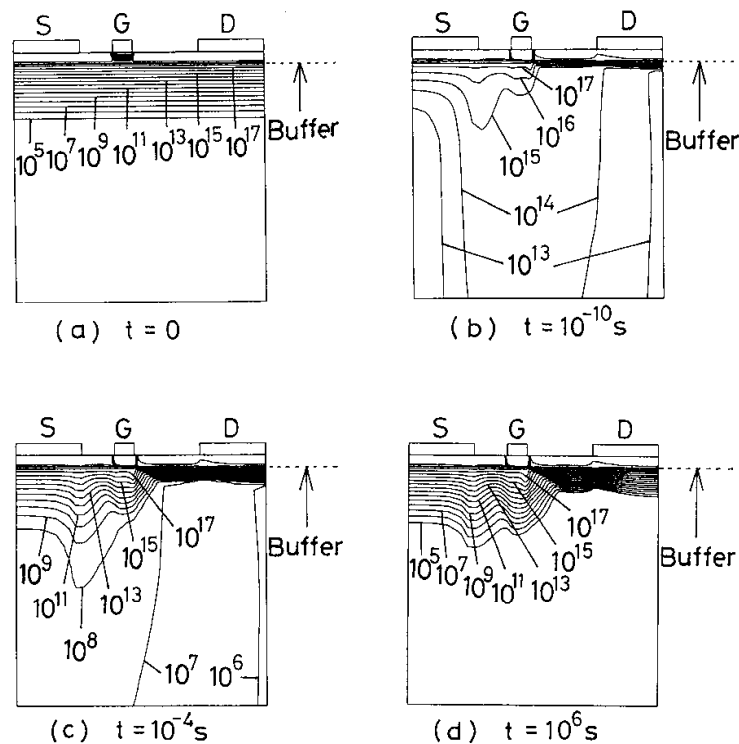


Fig. 3. Change of electron density profiles with time  $t$  when  $V_D$  is raised from 0 V to 20 V for the case of  $E_C - E_{DD} = 1.0$  eV, corresponding to Fig.2. (a) initial state ( $t = 0$ ), (b)  $t = 10^{-10}$  s, (c)  $t = 10^{-4}$  s, (d)  $t = 10^6$  s.

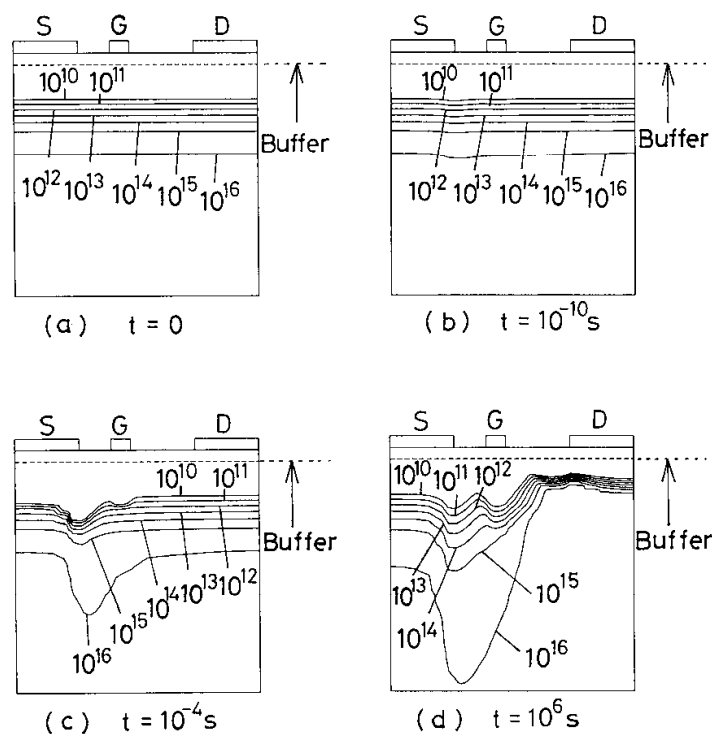


Fig. 4. Change of ionized deep-donor density  $N_{DD}^+$  profiles with time  $t$  when  $V_D$  is raised from 0 V to 20 V for the case of  $E_C - E_{DD} = 1.0$  eV, corresponding to Fig.2. (a) initial state ( $t = 0$ ), (b)  $t = 10^{-10}$  s, (c)  $t = 10^{-4}$  s, (d)  $t = 10^6$  s.



fact, from Figs.3(c) and 4(c), it is seen that electron densities in the buffer layer are decreasing and  $N_{DD}^+$  is decreasing particularly under the source-to-gate region. The undershoot or slight increase in  $I_D$  before reaching the steady state, which was observed in Fig.2, is regarded as a result of over capturing or due to electron emission by deep donors around the drain side of the gate region (see Figs.4(a) and (d)).

On the other hand, in the case when  $V_D$  is lowered, the response is simply understood by (captured) electron emission process of the deep donors. In fact, the current rise time is roughly consistent with the deep donor's electron-emission time constant given by  $1/e_{n,DD}$ , which becomes  $3.9 \times 10^{-5}$  s and  $9.8 \times 10^{-3}$  s for  $E_C - E_{DD} = 0.5$  eV and 1.0 eV, respectively. The time constant for  $E_C - E_{DD} = 1.7$  eV becomes quite long ( $> 10^{10}$  s), so that  $I_D$  remains at a low value even at  $t = 10^6$  s, as was seen in Fig.2.

Here, it should be mentioned that above drain lag phenomena (overshoot and undershoot behavior) are also reported experimentally in AlGaIn/GaN HEMTs (Binari et al., 2002; Meneghesso et al., 2004).

### 3.2 Gate lag and pulsed I-V curves

Next, we describe a case when the gate voltage  $V_G$  is also changed (from an off point). Fig.5 shows calculated turn-on characteristics of a normal AlGaIn/GaN HEMT when  $V_G$  is changed from the threshold voltage  $V_{th}$  ( $= -9.24$  V) to 0 V. Off-state drain voltage  $V_{Doff}$  is 20 V and the parameter is an on-state drain voltage  $V_{Don}$ .  $V_{th}$  is defined here as a gate voltage when  $I_D$  becomes  $5 \times 10^{-3}$  A/cm. Here,  $N_{DD} = 5 \times 10^{16}$  cm $^{-3}$ ,  $N_{DA} = 2 \times 10^{16}$  cm $^{-3}$  and  $E_C - E_{DD} = 1.0$  eV.  $V_{th}$  becomes rather deep because the current component via the buffer layer exists. The characteristics are similar to those shown in Fig.2 where  $V_D$  is lowered. However, as seen in the uppermost curve of Fig.5 ( $V_{Doff} = V_{Don} = 20$  V), some transients are observed when only  $V_G$  is changed. This indicates that gate lag as well as drain lag could occur due to deep levels in the buffer layer. We will describe below why the gate lag arises.

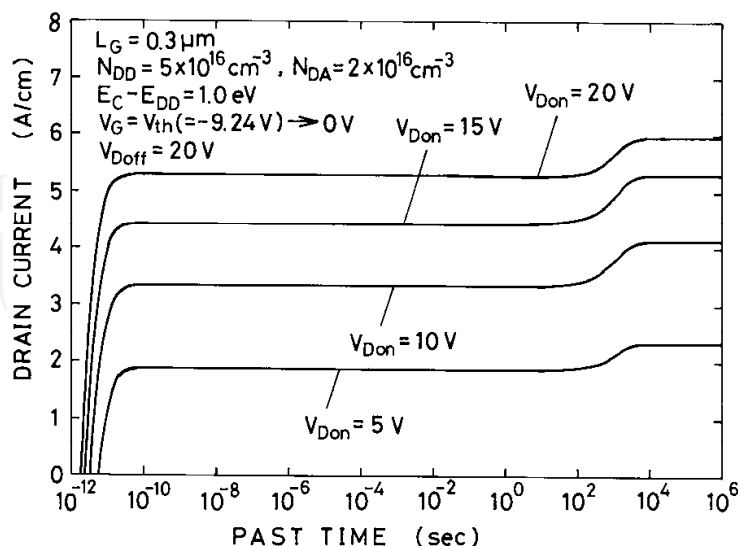


Fig. 5. Calculated turn-on characteristics of the normal AlGaIn/GaN HEMT when  $V_G$  is changed from threshold voltage  $V_{th}$  ( $= -9.24$  V) to 0 V, with on-state drain voltage  $V_{Don}$  as a parameter. Off-state drain voltage  $V_{Doff}$  is 20 V.  $L_{GD} = 1$   $\mu$ m and  $E_C - E_{DD} = 1.0$  eV.

Fig.6 shows a comparison of (a) conduction-band-edge energy profiles, (b) electron density profiles, and (c)  $N_{DD^+}$  profiles between the on state (left:  $V_D = 20$  V,  $V_G = 0$  V) and the off state (right:  $V_D = 20$  V,  $V_G = V_{th} = -9.24$  V). Note that only  $V_G$  is different here. From Fig.6(a), in the on state, some potential drops are observed between source and gate (and between gate and drain). The potential drop is given by  $I$  (current)  $\times R$  (resistance), and hence the large current and relatively large resistance become a cause of the visible potential drop. This indicates that source access resistance (and drain access resistance) is not negligible. It is understood that due to this potential drop at the source side, when  $V_G$  becomes negative and the channel is depleted, electrons under the gate are not all pushed into the source and drain electrodes, but can be injected into the buffer layer as seen in Fig.6(b). (Note that the energy barrier at the channel-buffer interface can be weakened under the gate when  $V_G$  becomes strongly negative.) These electrons are captured by deep donors, and hence  $N_{DD^+}$  decreases in the off state, as seen in Fig.6(c). Because of this increase in negative space

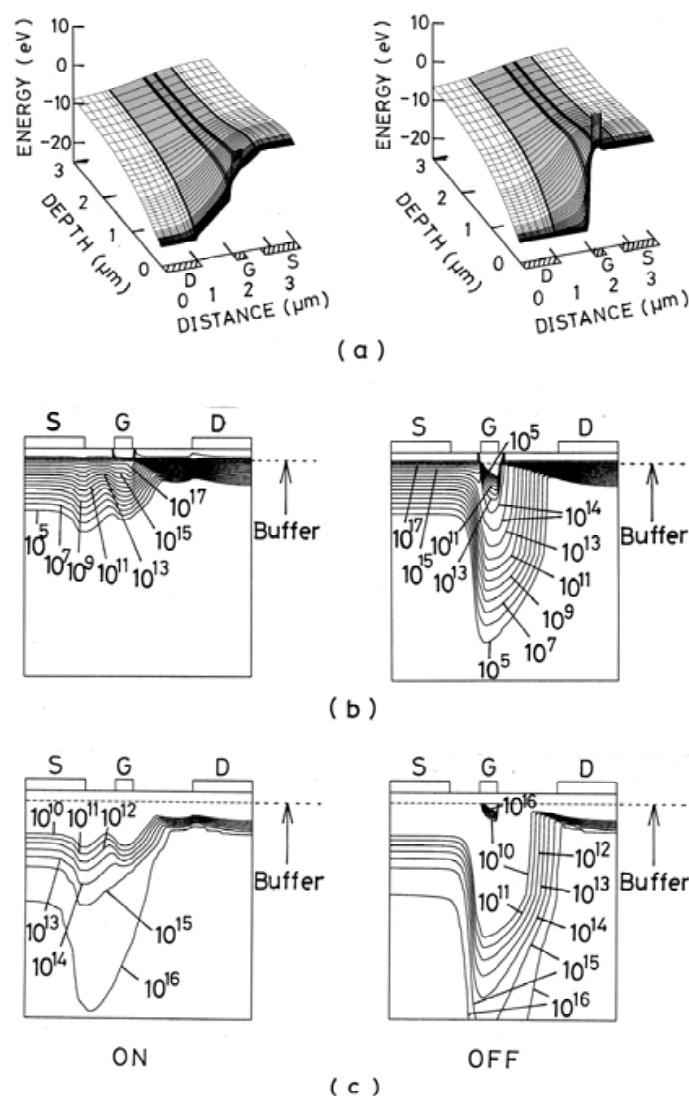


Fig. 6. (a) Conduction-band-edge energy profiles, (b) electron density profiles, and (c)  $N_{DD^+}$  profiles when only  $V_G$  is different. The left is for  $V_G = 0$  V and  $V_D = 20$  V (ON: steady state), and the right is for  $V_G = V_{th} = -9.24$  V and  $V_D = 20$  V (OFF: steady state).  $N_{DD} = 5 \times 10^{16} \text{ cm}^{-3}$ ,  $N_{DA} = 2 \times 10^{16} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0$  eV.



charges in the buffer layer, even if  $V_G$  is switched on,  $I_D$  remains at a low value until the deep donors begin to emit electrons, showing gate-lag behavior. It should be mentioned that this type of gate lag is not observed in the similar simulation for GaAs MESFETs with deep donors "EL2" and shallow acceptors in the substrate (Horio et al., 2000), where visible potential drops are not observed in the on state between source and gate. This is because the current density is relatively low and the parasitic resistance is low due to the higher electron mobility. Therefore, in the case of AlGaIn/GaN HEMTs, we can say that relatively high source access resistance is correlated to the gate lag. The high access resistance in AlGaIn/GaN HEMTs is considered problematic because it degrades the high-frequency performance (Palacios et al., 2005).

Next, we describe  $I$ - $V$  characteristics. Fig.7 shows calculated  $I_D$ - $V_D$  curves of the normal AlGaIn/GaN HEMT with a semi-insulating buffer layer, where  $N_{DD} = 5 \times 10^{16} \text{ cm}^{-3}$ ,  $N_{DA} = 2 \times 10^{16} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0 \text{ eV}$ . The solid line is the steady-state  $I$ - $V$  curve. In this figure, we plot by point (x) the drain current at  $t = 10^{-8} \text{ s}$  (after  $V_G$  is switched on) as a parameter of  $V_{Don}$  ( $V_D$ ). This is obtained from calculated turn-on characteristics like Fig.5, and hence this curve corresponds to a quasi-pulsed  $I$ - $V$  curve with pulse width of  $10^{-8} \text{ s}$ . (In this figure, for reference, we are also plotting other quasi-pulsed  $I$ - $V$  curves ( $\circ$ ,  $\Delta$ ) when only  $V_D$  is changed, which reflect overshoot and undershoot (cf. Fig.2).) It is seen that the drain currents in the pulsed  $I$ - $V$  curves are rather lower than those in the steady state, and the current reduction due to drain lag is regarded as predominant in this case ( $V_{Doff} = 40 \text{ V}$ ). This clearly indicates that the current collapse could occur due to the slow response of deep levels in the buffer layer. This type of current reduction (current collapse) is commonly observed experimentally in AlGaIn/GaN HEMTs.

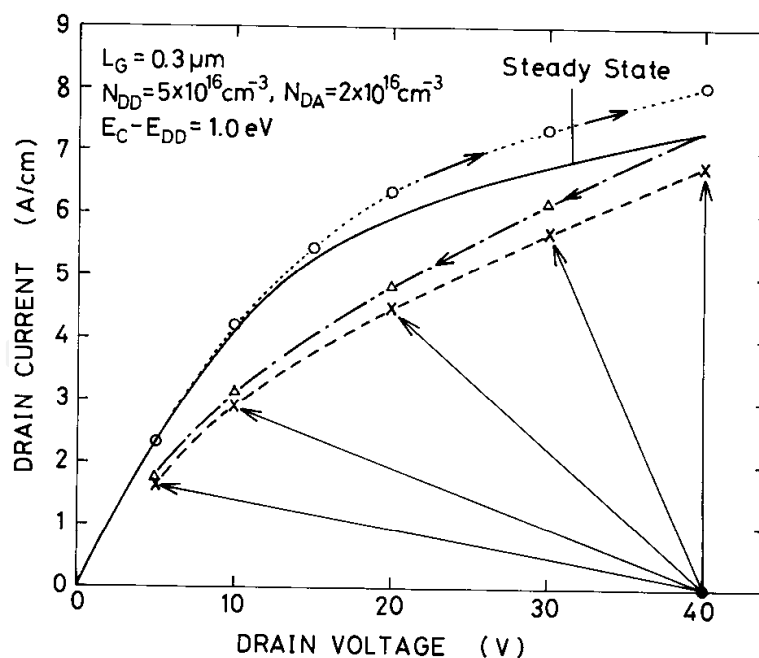


Fig. 7. Steady-state  $I$ - $V$  curve (solid line) and quasi-pulsed  $I$ - $V$  curves of normal AlGaIn/GaN HEMT, with  $L_{GD} = 1 \mu\text{m}$ ,  $N_{DD} = 5 \times 10^{16} \text{ cm}^{-3}$ ,  $N_{DA} = 2 \times 10^{16} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0 \text{ eV}$ . (x):  $V_{Doff} = 40 \text{ V}$  and  $V_{Goff} = V_{th}$  ( $t = 10^{-8} \text{ s}$ ), ( $\circ$ ):  $V_D$  is raised from  $0 \text{ V}$  ( $t = 10^{-9} \text{ s}$ ), ( $\Delta$ ):  $V_D$  is lowered from  $40 \text{ V}$  ( $t = 10^{-8} \text{ s}$ ).

### 3.3 Current collapse

In this section, we describe dependence of current collapse on the impurity densities in the buffer layer and on the off-state drain voltage.

#### 3.3.1 Dependence on deep-acceptor density

We have calculated dependence of drain-current responses and  $I$ - $V$  curves on impurity densities in the buffer layer, and found that these are essentially determined by the deep-acceptor density  $N_{DA}$  when  $N_{DD} > N_{DA}$  and  $E_C - E_{DD}$  is the same. For example,  $I$ - $V$  curves for  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$  and  $N_{DA} = 2 \times 10^{16} \text{ cm}^{-3}$  are almost the same as those for  $N_{DD} = 5 \times 10^{16} \text{ cm}^{-3}$  and  $N_{DA} = 2 \times 10^{16} \text{ cm}^{-3}$  shown in Fig.7 (The difference is 2 ~ 3 %). This is because when  $N_{DD} > N_{DA}$ , the ionized deep-donor density  $N_{DD}^+$  becomes nearly equal to  $N_{DA}$  under equilibrium, and the space-charge region in the buffer layer consists of negative charges due to ionized deep acceptors. Therefore, we will show  $N_{DA}$  dependence of the characteristics.

Fig.8 shows calculated  $I_D$ - $V_D$  curves of normal AlGaIn/GaN HEMTs with different  $N_{DA}$  ( $5 \times 10^{15} \text{ cm}^{-3}$ ,  $10^{17} \text{ cm}^{-3}$ ) in the buffer layer. Here,  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0 \text{ eV}$ . The solid lines are steady-state  $I$ - $V$  curves, and the dashed lines (x) are quasi-pulsed  $I$ - $V$  curves with pulse width of  $10^{-8} \text{ s}$ , which are obtained from calculated turn-on characteristics, as described before. It is seen that for lower  $N_{DA}$ , the steady-state drain currents are higher, and the saturation behavior is poor. This is because a barrier between the channel and the buffer is less steep and the current component via the buffer layer becomes larger. This type of short-channel effect is recently discussed in (Uren et al., 2006). Combined with Fig.7, it is also clearly seen that the current collapse is more pronounced for higher  $N_{DA}$ . This is because the ionized deep-donor density  $N_{DD}^+$ , which acts as an electron trap, is higher for higher  $N_{DA}$ , and hence the trapping effects (or the resulting current collapse) are more

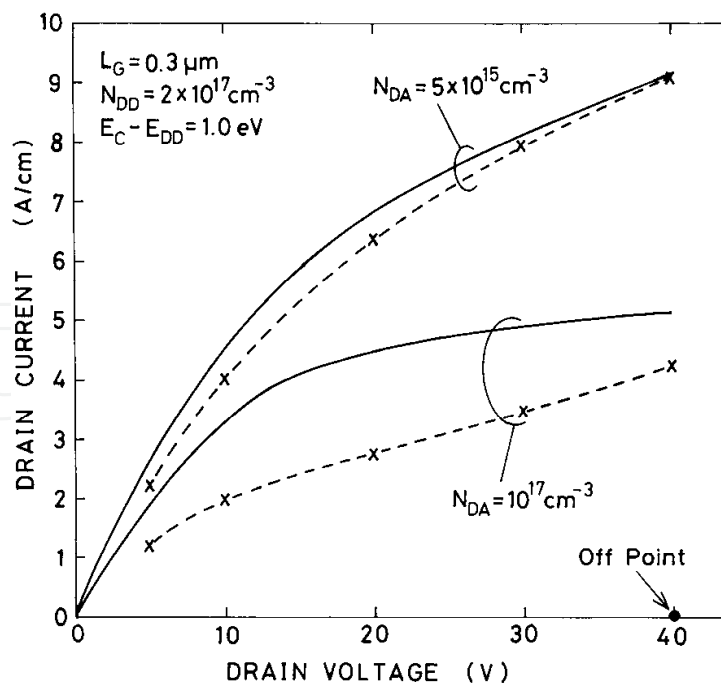


Fig. 8. Steady-state  $I$ - $V$  curves ( $V_G = 0 \text{ V}$ ; solid lines) and quasi-pulsed  $I$ - $V$  curves (x;  $t = 10^{-8} \text{ s}$ ) for normal AlGaIn/GaN HEMTs with different  $N_{DA}$ . Initial point is shown by (●).  $L_{GD} = 1 \text{ μm}$ ,  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0 \text{ eV}$ .

significant for higher  $N_{DA}$ . Here, it should be mentioned that for lower  $N_{DA}$ , the current collapse could be reduced, but the threshold voltage shifts toward negative bias due to the higher buffer current, although this current should become small when  $L_G$  is long. Therefore, there may be a trade-off relationship between reducing current collapse and obtaining sharp current cutoff.

### 3.3.2 Dependence on off-state drain voltage

Finally, we describe dependence of current collapse on the off-state drain voltage  $V_{Doff}$ . Fig.9 shows a calculated steady-state  $I_D$ - $V_D$  curve (solid line) and quasi-pulsed  $I$ - $V$  curves (x; with pulse width of  $10^{-8}$  s) which are derived from calculated turn-on characteristics. The parameter is  $V_{Doff}$ . Here,  $L_{GD} = 1.5 \mu\text{m}$ ,  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0$  eV. It is seen that for higher  $V_{Doff}$ , the drain currents in the pulsed  $I$ - $V$  curves are lower at a given  $V_D$ . Therefore, it can be said that the current collapse is more pronounced when  $V_{Doff}$  is higher. Although some current reduction is seen when only  $V_G$  is changed (gate lag), the current reduction due to the change of  $V_D$  (drain lag) is regarded as predominant for the cases of higher  $V_{Doff}$ .

Fig.10 shows (a) electron density profiles and (b)  $N_{DD}^+$  profiles in the off state for the two cases. The left is for  $V_{Doff} = 20$  V ( $V_G = V_{th} = -7.50$  V) and the right is for  $V_{Doff} = 80$  V ( $V_G = V_{th} = -8.56$  V). It is seen that for higher  $V_{Doff}$ , electron densities in the buffer layer are higher under the gate and the gate-to-drain region, because electrons are injected into the buffer layer by the applied drain voltage. These electrons are captured by the deep donors, and hence  $N_{DD}^+$  decreases more heavily, as seen in Fig.10(b). Hence, when  $V_G$  is switched on and  $V_D$  is lowered from higher  $V_{Doff}$ , the drain current remains at a lower value. Therefore, the current collapse is more pronounced for higher  $V_{Doff}$ . The tendency shown in Fig.9 is also reported experimentally in AlGaIn/GaN HEMTs (Koudymov et al., 2003).

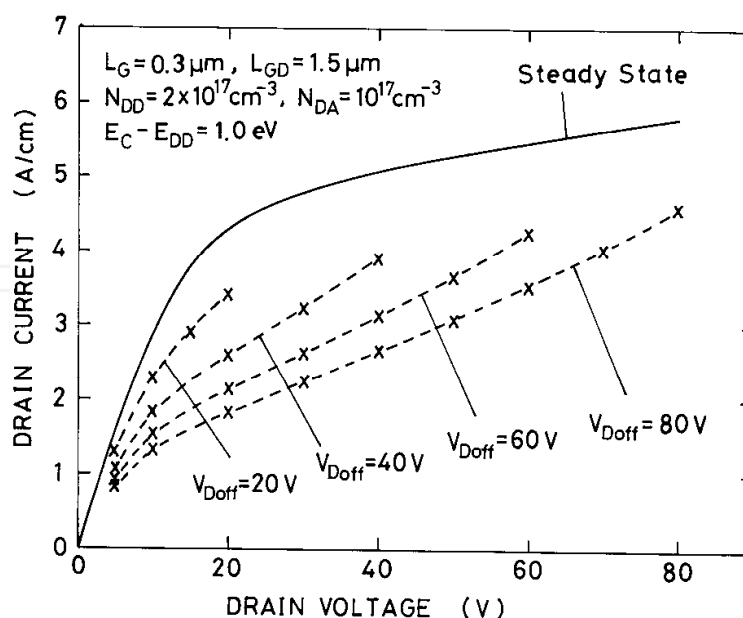


Fig. 9. Steady-state  $I$ - $V$  curve ( $V_G = 0$  V; solid line) and quasi-pulsed  $I$ - $V$  curves (x;  $t = 10^{-8}$  s) for normal AlGaIn/GaN HEMT, with off-state drain voltage  $V_{Doff}$  as a parameter.  $L_{GD} = 1.5 \mu\text{m}$ ,  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0$  eV.

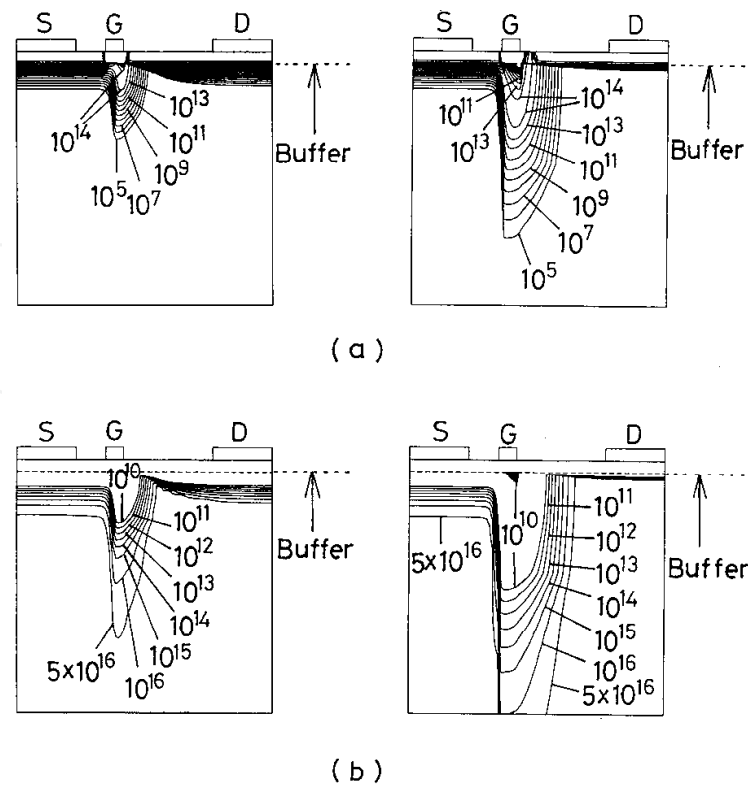


Fig. 10. (a) Electron density profiles and (b)  $N_{DD^+}$  profiles in the off state. The left is for  $V_{Doff} = 20$  V and the right is for  $V_{Doff} = 80$  V.  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 1.0$  eV.

## 4. Effects of Field Plate

### 4.1 Drain lag

Next, we describe effects of a field plate. First, we discuss about the drain lag. Fig.11 shows a comparison of calculated drain-current responses of AlGaIn/GaN HEMTs ( $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$ ,  $E_C - E_{DD} = 0.5$  eV) when  $V_D$  is lowered abruptly from  $V_{Dini}$  (40 V) to  $V_{Dfin}$  abruptly, where the gate voltage  $V_G$  is kept constant at 0 V. Fig.11(a) is for the case without a field plate ( $L_{FP} = 0$ ) and Fig.11(b) is for the field-plate structure ( $L_{FP} = 1 \mu\text{m}$ ). In Fig.11, the thickness of SiN layer  $d$  is  $0.03 \mu\text{m}$ . In both cases with and without a field plate, the drain currents remain at low values for some periods and begin to increase slowly, showing drain-lag behavior. It is understood that the drain currents begin to increase when the deep donors in the buffer layer begin to emit electrons. This electron emission occurs because for higher  $V_D$ , more electrons are injected into the buffer layer and captured by deep donors, leading to a more negatively charged buffer layer. It is seen that the change of drain current is smaller for the cases with a field plate, indicating that the drain lag is smaller for the field-plate structure. We will discuss below why the drain lag or the trapping effect becomes smaller in the field-plate structure.

Fig.12 shows (a) electron density profiles and (b) ionized deep-donor density  $N_{DD^+}$  profiles at  $V_G = 0$  V and  $V_D = 40$  V for the AlGaIn/GaN HEMTs. The left is for the structure without a field plate, and the right is for the field-plate structure. In Fig.12(a), we see that for the structure without a field plate, electrons are injected deeper into the buffer layer under the

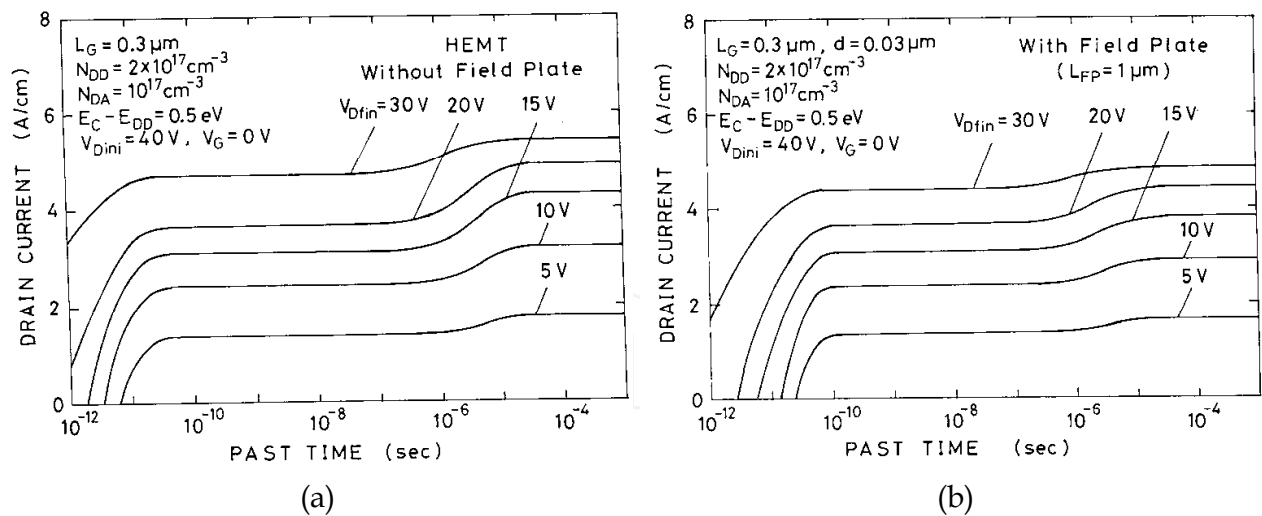


Fig. 11. Calculated drain-current responses of AlGaIn/GaN HEMTs when  $V_D$  is lowered abruptly from 40 V to  $V_{Dfin}$ , while  $V_G$  is kept constant at 0 V.  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 0.5 \text{ eV}$ . (a) Without a field plate, (b) with 1  $\mu\text{m}$ -length field plate.

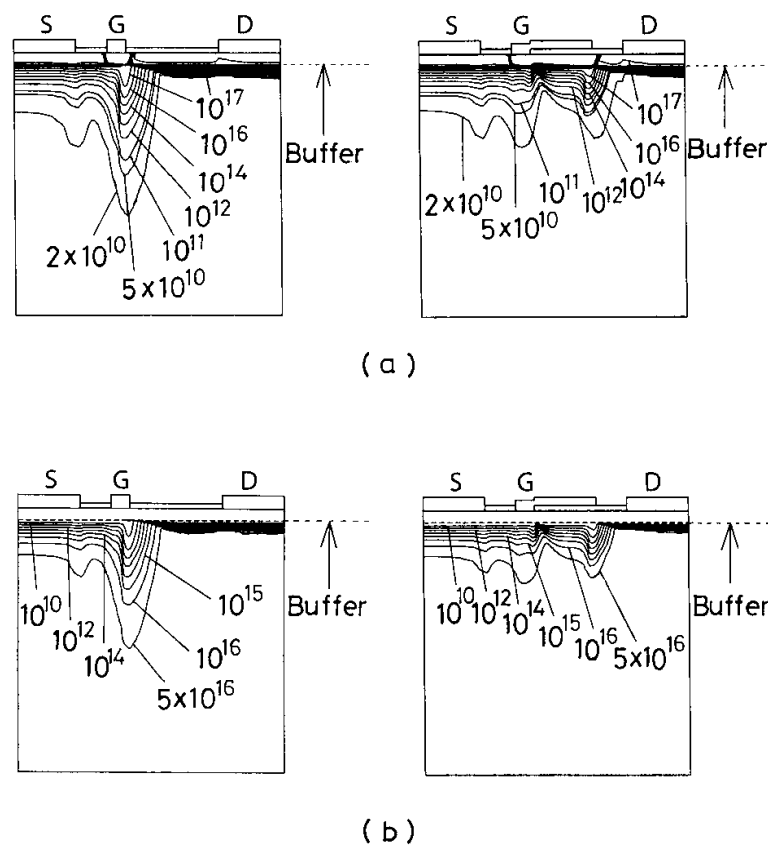


Fig. 12. (a) Electron density profiles and (b) ionized deep-donor density  $N_{DD}^+$  profiles at  $V_G = 0 \text{ V}$  and  $V_D = 40 \text{ V}$  for AlGaIn/GaN HEMTs.  $d = 0.03 \mu\text{m}$ .  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 0.5 \text{ eV}$ . The left is for the case without a field plate, and the right is for the field-plate structure ( $L_{FP} = 1 \mu\text{m}$ ).

gate region. These electrons are captured by the deep donors, and hence  $N_{DD}^+$  decreases there as seen in Fig.12(b). As mentioned before, when  $V_D$  is lowered abruptly, the drain currents remain at low values for some periods and begin to increase slowly as the deep donors begin to emit electrons (and  $N_{DD}^+$  increases), resulting in the drain lag. In the case of field-plate structure, as seen in Fig.12(a), electrons are injected into the buffer layer under the drain edge of field plate as well as under the gate. But the overall injection depth is not so deep as compared to the case without a field plate. Hence, the change of  $N_{DD}^+$  by capturing electrons is smaller for the field-plate structure as seen in Fig.12(b). This occurs because the electric fields at the drain edge of the gate become weaker by introducing a field plate, as shown in Fig.13. (Note that in the field-plate structure, the electric fields at the drain edge of the field plate can be strong for thin  $d$ .) Therefore, the drain lag becomes smaller for the field-plate structure.

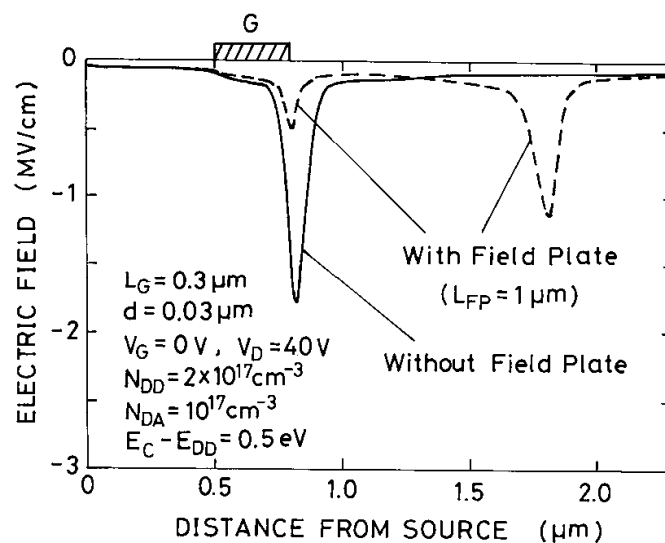


Fig. 13. Comparison of longitudinal electric field profiles at the channel side of heterojunction in AlGaIn/GaN HEMTs with and without a field plate.  $V_G = 0$  V and  $V_D = 40$  V.  $d = 0.03$   $\mu\text{m}$ .  $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{DA} = 10^{17} \text{ cm}^{-3}$  and  $E_C - E_{DD} = 0.5$  eV.

#### 4.2 Pulsed $I$ - $V$ curves and current collapse

Next, we have calculated a case when  $V_G$  is also changed from an off point.  $V_G$  is changed from the threshold voltage  $V_{th}$  to 0 V, and  $V_D$  is changed from  $V_{Dini}$  (40 V) to  $V_{Don}$  (on-state drain voltage). The characteristics become similar to those in Fig.11, although some transients arise when only  $V_G$  is changed (gate lag). From the transient characteristics, we obtain quasi-pulsed  $I$ - $V$  curves.

Fig.14 shows calculated drain current  $I_D$  - drain voltage  $V_D$  curves of AlGaIn/GaN HEMTs. Fig.14(a) is for the structure without a field plate, and Fig.14(b) is for the field-plate structure ( $L_{FP} = 1$   $\mu\text{m}$ ). The solid lines are steady-state  $I$ - $V$  curves. In these figures, we plot by ( $\Delta$ ) the drain current at  $t = 10^{-8}$  s after  $V_D$  is lowered. This is obtained from the previous transient characteristics (Fig.11), and this curve (dashed line) is regarded as a quasi-pulsed  $I$ - $V$  curve with pulse width of  $10^{-8}$  s. This reduction in the drain current indicates the drain-lag behavior. In these figures, we also plot by (x) another pulsed  $I$ - $V$  curve when  $V_G$  is switched



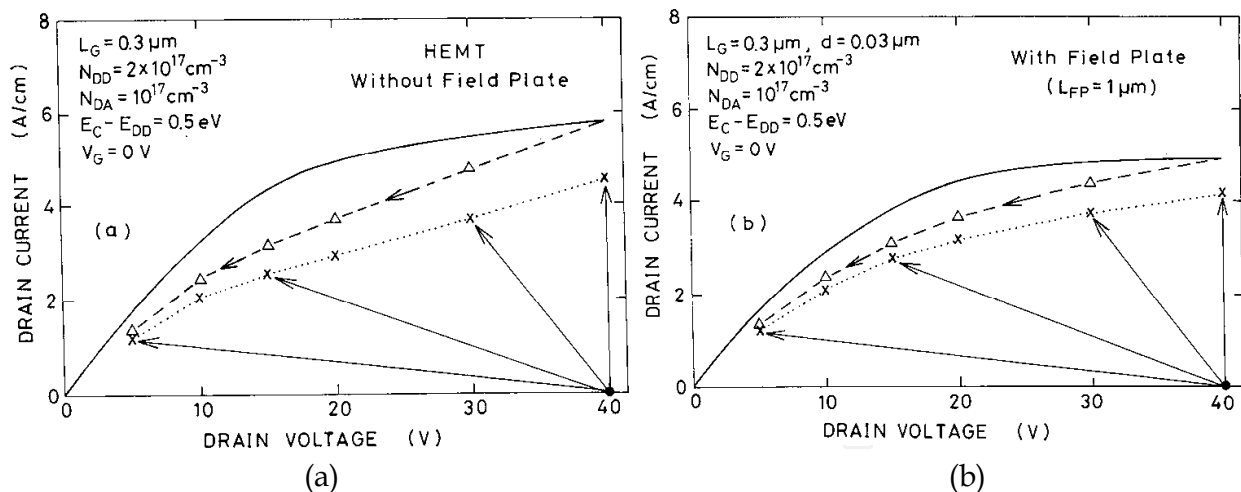


Fig.14. Steady-state  $I$ - $V$  curves ( $V_G = 0 \text{ V}$ ; solid lines) and quasi-pulsed  $I$ - $V$  curves ( $\Delta$ ,  $x$ ) of AlGaIn/GaN HEMTs. (a) Without a field plate, (b) with  $1 \mu\text{m}$ -length field plate. ( $\Delta$ ): Only  $V_D$  is changed from  $40 \text{ V}$  ( $t = 10^{-8} \text{ s}$ ), ( $x$ ):  $V_D$  is lowered from  $40 \text{ V}$  and  $V_G$  is changed from  $V_{th}$  to  $0 \text{ V}$  ( $t = 10^{-8} \text{ s}$ ).

on from  $V_{th}$  to  $0 \text{ V}$ . The drain current in this case is further reduced, indicating gate-lag and current collapse behavior. The current collapse is a combined effect of drain lag and gate lag. By comparing the cases with and without a field plate, we can definitely say that the lag phenomena (drain lag, gate lag) and current collapse become smaller for the field-plate structure.

#### 4.3 Dependence on SiN layer thickness

Finally, we have studied how the lag phenomena and current collapse depend on the field-plate length  $L_{FP}$  and the SiN layer thickness  $d$ . We have found that the lag phenomena and current collapse become smaller when  $L_{FP}$  becomes longer in the range from  $0$  to  $1 \mu\text{m}$ . This may be easily understood, because trapping effects should be reduced for longer  $L_{FP}$ . Hence, we will here focus on the dependence of lag phenomena and current collapse on the SiN layer thickness  $d$ .

Fig.15 shows drain-current reduction rate  $\Delta I_D / I_D$  ( $\Delta I_D$ : current reduction,  $I_D$ : steady-state current) due to current collapse, drain lag or gate lag as a function of  $d$ , where  $L_G = 0.3 \mu\text{m}$  and  $L_{FP} = 1 \mu\text{m}$ . Here  $d = 0$  corresponds to a case of  $L_G = 1.3 \mu\text{m}$  without a field plate. The data in Fig.15 are for the field-plate structures, except for  $d = 0$ . When  $d$  is thick, the current collapse and lag phenomena are relatively large. As  $d$  becomes thinner, the current collapse and lag phenomena become smaller. This is because the buffer-trapping effects are reduced in the field-plate structure, as described in sections 4.1 and 4.2. However, the rates of current collapse and drain lag increase when  $d$  becomes very thin. This is understood that for very thin  $d$ , the electric field at the drain edge of the field plate becomes very strong, and electrons are injected deeper into the buffer layer under the field-plate region, contributing to the current collapse and drain lag. When  $d = 0$  ( $L_G = 1.3 \mu\text{m}$ ), that is, without a field plate, the current collapse becomes rather large. From Fig.15, we can say that there is an optimum thickness of SiN layer to minimize the buffer-related current collapse and drain lag in AlGaIn/GaN HEMTs.

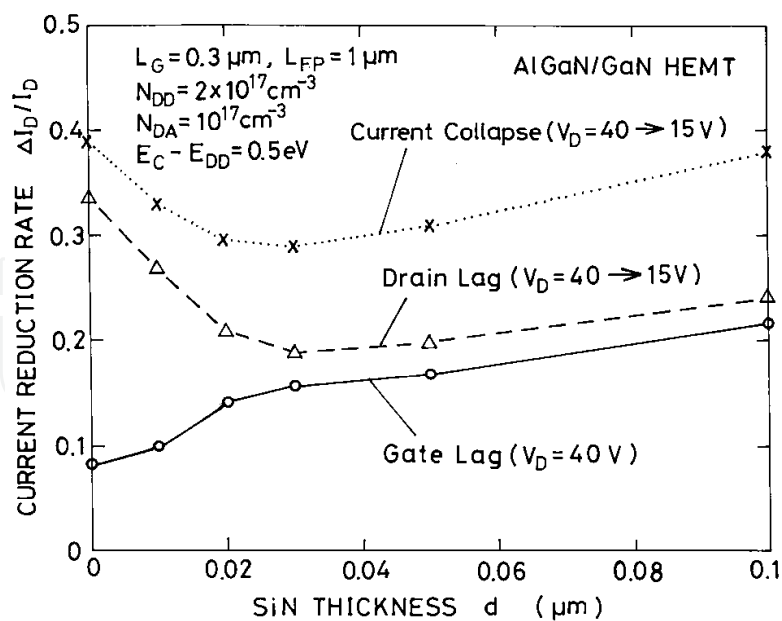


Fig. 15. Current reduction rate  $\Delta I_D/I_D$  due to current collapse, drain lag or gate lag for field-plate AlGaIn/GaN HEMTs as a function of SiN thickness  $d$ .  $L_{FP} = 1 \mu\text{m}$ .

## 5. Conclusion

Two-dimensional transient analyses of AlGaIn/GaN HEMTs have been performed in which the three level compensation model is adopted for the buffer layer, where a shallow donor, a deep donor and a deep acceptor are considered. Quasi-pulsed  $I$ - $V$  curves have been derived from the transient characteristics, and compared with steady-state  $I$ - $V$  curves. It has been shown that the lag phenomena and current collapse could be reproduced, as in GaN MESFETs (Horio et al., 2005).

When the drain voltage is lowered abruptly, the drain currents remain at low values for some periods and begin to increase slowly as the deep donors begin to emit electrons, showing drain-lag behavior. As compared with the case of GaN MESFETs, relatively large gate lag due to buffer traps could arise, and it is correlated to relatively high source access resistance in AlGaIn/GaN HEMTs. Both the drain lag and the gate lag become causes of current collapse. The current collapse has been shown to be more pronounced when the deep-acceptor density in the buffer layer is higher and when an off-state drain voltage is higher, because the trapping effects become more significant. The drain lag could be a major cause of current collapse in the case of higher off-state drain voltage.

It is concluded that to minimize current collapse in AlGaIn/GaN HEMTs, an acceptor density in the buffer layer should be made low, although the buffer current becomes large and short-channel effects become significant when the gate length is short. Some ways to reduce the short-channel effects such as using a heterojunction buffer may be needed. Here, it should be mentioned that to clarify surface-state effects in AlGaIn/GaN HEMTs, which are not considered here, is an important task yet to be done.

Effects of introducing a field plate have also been studied. It has been shown that the drain lag is reduced by introducing a field plate because the electric field at the drain edge of the gate becomes weaker and electron injection into the buffer layer is reduced, resulting in the

smaller buffer-trapping effects. It has also been shown that the buffer-related current collapse and gate lag are reduced in the field-plate structure. The dependence of lag phenomena and current collapse on SiN layer thickness has also been studied, indicating that there is an optimum thickness of SiN layer to minimize the buffer-related current collapse and drain lag in AlGaIn/GaN HEMTs.

## 6. References

- Ando, Y.; Okajima, Y.; Miyamoto, H.; Nakayama, T.; Inoue, T. & Kuzuhara, M. (2003). 10-W/mm AlGaIn-GaN HFET with a field modulating plate. *IEEE Electron Device Lett.*, Vol.24, No.5, pp.289-91.
- Binari, S. C.; Klein, P. B. & Kazior, T. E. (2002). Trapping effects in GaN and SiC Microwave FETs. *Proc. IEEE*, Vol.90, pp.1048-1058.
- Braga, N.; Mickevicius, R.; Gaska, R.; Shur, M. S.; Khan, M. A. & Simin, G. (2004). Simulation of gate lag and current collapse in GaN heterojunction field effect transistors. *Proceedings of IEEE CSIC Symp.*, pp.287-290.
- Daumiller, I.; Theron, D.; Gaquiere, C.; Vescan, A.; Dietrich, R.; Wieszt, A.; Leiter, H.; Veturly, R.; Mishra, U. K.; Smorchkova, I. P.; Keller, S.; Nguyen, N. X.; Nguyen, C. & Kohn, E. (2001). Current instabilities in GaN-based devices. *IEEE Electron Device Lett.*, Vol.22, No.2, pp.62-64.
- Desmaris, V.; Rudzinski, M.; Rorsman, N.; Hageman, P. R.; Larsen, P. K.; Zirath, H.; Rodle, T. C. & Jos, H. F. F. (2006). Comparison of the dc and microwave performance of AlGaIn/GaN HEMTs grown on SiC by MOCVD with Fe-doped or unintentionally doped GaN buffer layer. *IEEE Trans. Electron Devices*, Vol.53, No.9, pp.2413-2417.
- Higashiwaki, M.; Matsui, T. & Mimura, T. (2006). AlGaIn/GaN MIS-HFETs with  $f_T$  of 163 GHz using CAT-CVD SiN gate-insulating and passivation layers. *IEEE Electron Device Lett.*, Vol.27, No.1, pp.16-18.
- Horio, K. & Fuseya, Y. (1994). Two-dimensional simulations of drain-current transients in GaAs MESFET's with semi-insulating substrates compensated by deep levels. *IEEE Trans. Electron Devices*, Vol.41, No.8, pp.1340-1346.
- Horio, K.; Wakabayashi, A. & Yamada, T. (2000). Two-dimensional analysis of substrate-trap effects on turn-on characteristics in GaAs MESFET's. *IEEE Trans. Electron Devices*, Vol.47, No.3, pp.617-624.
- Horio, K.; Yonemoto, K.; Takayanagi, H. & Nakano, H. (2005). Physics-based simulation of buffer-trapping effects on slow current transients and current collapse in GaN field effect transistors. *J. Appl. Phys.*, Vol.98, No.12, pp.124502 1-7.
- Horio, K. & Nakajima, A. (2008). Physical mechanism of buffer-related current transients and current slump in AlGaIn/GaN high electron mobility transistors. *Jpn. J. Appl. Phys.*, Vol.47, No.5, pp.3428-3433.
- Karmalkar, S. & Mishra, U. K. (2001). Enhancement of breakdown voltage in AlGaIn/GaN high electron mobility transistors using a field plate. *IEEE Trans. Electron Devices*, Vol.48, No.8, pp.1515-1521.
- Khan, M. A.; Shur, M. S.; Chen, Q. C. & Kuznia, J. N. (1994). Current/voltage characteristics collapse in AlGaIn/GaN heterostructure insulated gate field effect transistors at high drain bias. *Electron Lett.*, Vol.30, pp.2175-2176.

- Klein, P. B.; Freitas, Jr., J. A.; Binari, S. C. & Wickenden, A. E. (1999). Observation of deep traps responsible for current collapse in GaN metal-semiconductor field-effect transistors. *Appl. Phys. Lett.*, Vol.75, No.25, pp.4016-4018.
- Koley, G.; Tilak, V.; Eastman, L. F. & Spencer, M. G. (2003). Slow transients observed in AlGaIn/GaN HFETs: Effects of SiNx passivation and UV illumination. *IEEE Trans. Electron Devices*, Vol.50, No.4, pp.886-893.
- Koudymov, A.; Simin, G.; Khan, M. A.; Tarakji, A.; Gaska, R. & Shur, M. S. (2003). Dynamic current-voltage characteristics of III-N HFETs. *IEEE Electron Device Lett.*, Vol.24, pp.680-682.
- Koudymov, A.; Adivarahan, V.; Yang, J.; Simon, G. & Khan, M. A. (2005). Mechanism of current collapse removal in field-plated nitride HFETs. *IEEE Electron Device Lett.* Vol.26, pp.704-706.
- Kruppa, W.; Binari, S. C. & Doverspike, K. (1995). Low-frequency dispersion characteristics of GaN HFETs. *Electron. Lett.*, Vol.31, pp.1951-1952.
- Meneghesso, G.; Verzellesi, G.; Pierobon, R.; Rarnpazzo, F.; Chini, A.; Mishra, U. K.; Canali, C. & Zanoni, E. (2004). Surface-related drain current dispersion effects in AlGaIn/GaN HEMTs. *IEEE Trans. Electron Devices*, Vol.51, pp.1554-1561.
- Mishra, U. K.; Shen, L.; Kazior, T. E. & Wu, Y.-F. (2008). GaN-based RF power devices and amplifiers. *Proc. IEEE*, Vol.96, No.2, pp.287-305.
- Mizutani, T.; Ohno, Y.; Akita, M.; Kishimoto, S. & Maezawa, K. (2003). A study on current collapse in AlGaIn/GaN HEMTs induced by bias stress. *IEEE Trans. Electron Devices*, Vol.50, No.10, pp.2015-2020.
- Morkoc, H. (1999). *Nitride Semiconductors and Devices*, Springer-Verlag.
- Nakajima, A.; Itagaki, K. & Horio, K. (2009). Reduction of buffer-related current collapse in field-plate AlGaIn/GaN HEMTs. *phys. stat. soli (c)*, Vol.6, No.S2, pp.S929-S932.
- Pala, N.; Hu, X.; Deng, J.; Yang, J.; Koudymov, A.; Shur, M. S. & Simin, G. (2008). Drain-to-gate field engineering for improved frequency response of GaN-based HEMTs. *Solid-State Electron.*, Vol.52, No.8, pp.1217-1220.
- Palacios, T.; Rajan, S.; Chakraborty, A.; Heikman, S.; Keller, S.; DenBaars, S. P. & Mishra, U. K. (2005). Influence of the dynamic access resistance in the  $g_m$  and  $f_T$  linearity of AlGaIn/GaN HEMTs. *IEEE Trans. Electron Devices*, Vol.52, No.10, pp.2117-2123.
- Saito, W.; Kuraguchi, M.; Takada, Y.; Tuda, K.; Omura, I. & Ogura, T. (2005). Design optimization of high breakdown voltage AlGaIn-GaN power HEMT on an insulating substrate for  $R_{ONA}-V_B$  tradeoff characteristics. *IEEE Trans. Electron Devices*, Vol.52, No.1, pp.106-111.
- Tirado, J.; Sanchez-Rojas, J. L. & Izpura, J. I. (2007). Trapping Effects in the transient response of AlGaIn/GaN HEMT devices. *IEEE Trans. Electron Devices*, Vol.54, pp.410-417.
- Uren, M. J.; Nash, K. J.; Balmer, R. S.; Martin, T.; Morvan, E.; Caillas, N.; Delage, S. L.; Ducatteau, D.; Grimbert, B. & Jaeger, J. C. De (2006). Punch-through in short-channel AlGaIn/GaN HFETs. *IEEE Trans. Electron Devices*, Vol.53, No.2 pp.395-398.
- Vetury, R.; Zhang, N. Q.; Keller, S. & Mishra, U. K. (2001). The impact of surface states on the dc and RF characteristics of AlGaIn-GaN HFETs. *IEEE Trans. Electron Devices*, Vol.48, No.3, pp.560-566.

- Wu, Y.-F.; Saxler, A.; Moore, M.; Smith, R. P.; Sheppard, S.; Chavarkar, P. M.; Wisleder, T.; Mishra, U. K. & Parikh, P. (2004). 30 W/mm GaN HEMT by field plate optimization. IEEE Electron Device Lett., Vol.23, No.3, pp.117-119.
- Xing, H. X.; Dora, Y.; Chini, A.; Heikman, S.; Keller, S. & Mishra, U. K. (2004). High breakdown voltage AlGaIn-GaN HEMTs achieved by multiple field plates. IEEE Electron Device Lett., Vol.25, No.4, pp.161-163.

IntechOpen

IntechOpen



## **Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems**

Edited by Moumita Mukherjee

ISBN 978-953-307-031-5

Hard cover, 642 pages

**Publisher** InTech

**Published online** 01, March, 2010

**Published in print edition** March, 2010

This book is planned to publish with an objective to provide a state-of-the-art reference book in the areas of advanced microwave, MM-Wave and THz devices, antennas and system technologies for microwave communication engineers, Scientists and post-graduate students of electrical and electronics engineering, applied physicists. This reference book is a collection of 30 Chapters characterized in 3 parts: Advanced Microwave and MM-wave devices, integrated microwave and MM-wave circuits and Antennas and advanced microwave computer techniques, focusing on simulation, theories and applications. This book provides a comprehensive overview of the components and devices used in microwave and MM-Wave circuits, including microwave transmission lines, resonators, filters, ferrite devices, solid state devices, transistor oscillators and amplifiers, directional couplers, microstripeline components, microwave detectors, mixers, converters and harmonic generators, and microwave solid-state switches, phase shifters and attenuators. Several applications area also discusses here, like consumer, industrial, biomedical, and chemical applications of microwave technology. It also covers microwave instrumentation and measurement, thermodynamics, and applications in navigation and radio communication.

### **How to reference**

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Kazushige Horio (2010). Analysis of Parasitic Effects in AlGaIn/GaN HEMTs, Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems, Moumita Mukherjee (Ed.), ISBN: 978-953-307-031-5, InTech, Available from: <http://www.intechopen.com/books/advanced-microwave-and-millimeter-wave-technologies-semiconductor-devices-circuits-and-systems/analysis-of-parasitic-effects-in-aigan-gan-hemts>

**INTECH**  
open science | open minds

### **InTech Europe**

University Campus STeP Ri  
Slavka Krautzeka 83/A  
51000 Rijeka, Croatia  
Phone: +385 (51) 770 447  
Fax: +385 (51) 686 166  
[www.intechopen.com](http://www.intechopen.com)

### **InTech China**

Unit 405, Office Block, Hotel Equatorial Shanghai  
No.65, Yan An Road (West), Shanghai, 200040, China  
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元  
Phone: +86-21-62489820  
Fax: +86-21-62489821



© 2010 The Author(s). Licensee IntechOpen. This chapter is distributed under the terms of the [Creative Commons Attribution-NonCommercial-ShareAlike-3.0 License](https://creativecommons.org/licenses/by-nc-sa/3.0/), which permits use, distribution and reproduction for non-commercial purposes, provided the original is properly cited and derivative works building on this content are distributed under the same license.

IntechOpen

IntechOpen